CMOS, 2.5 Ω Low Voltage, Triple/Quad SPDT Switches

ADG733/ADG734

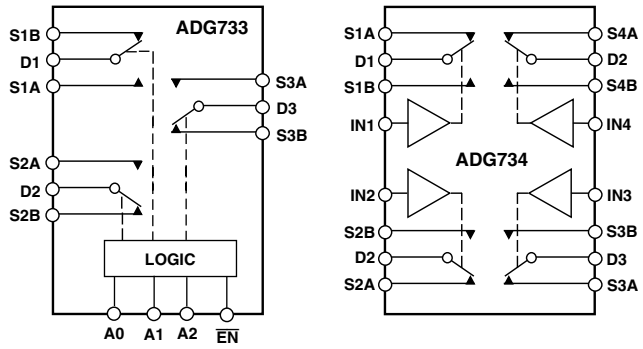
FEATURES

1.8 V to 5.5 V Single Supply
±2.5 V Dual Supply
2.5 Ω On Resistance
0.5 Ω On Resistance Flatness
100 pA Leakage Currents
19 ns Switching Times
Triple SPDT: ADG733
Quad SPDT: ADG734
Small TSSOP and QSOP Packages
Low Power Consumption
TTL/CMOS Compatible Inputs

APPLICATIONS

Data Acquisition Systems
Communication Systems
Relay Replacement
Audio and Video Switching
Battery Powered Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A "1" INPUT LOGIC

GENERAL DESCRIPTION

The ADG733 and ADG734 are low voltage, CMOS devices comprising three independently selectable SPDT (single pole, double throw) switches and four independently selectable SPDT switches respectively.

Low power consumption and operating supply range of 1.8 V to 5.5 V and dual ±2.5 V make the ADG733 and ADG734 ideal for battery powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. An $\overline{EN}$ input on the ADG733 is used to enable or disable the device. When disabled, all channels are switched OFF.

These 2–1 multiplexers/SPDT switches are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, high signal bandwidths, and low leakage currents. On resistance is in the region of a few ohms, is closely matched between switches, and is very flat over the full signal range. These parts can operate equally well in either direction and have an input signal range that extends to the supplies.

The ADG733 is available in small TSSOP and QSOP packages, while the ADG734 is available in a small TSSOP package.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Operation. The ADG733 and ADG734 are fully specified and guaranteed with 3 V and 5 V single supply rails and ±2.5 V dual supply rails.
2. Low On Resistance (2.5 Ω typical)
3. Low Power Consumption (<0.01 μW)
4. Guaranteed Break-Before-Make Switching Action

REV. A

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ADG733/ADG734–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	4.5	5.0	Ω max	Test Circuit 1
On Resistance Match between		0.1	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 1 V, or 4.5 V;
	±0.1	±0.5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	19		ns typ	R_L = 300 Ω, C_L = 35 pF;
		34	ns max	V_S = 3 V, Test Circuit 4
t_{OFF}	7		ns typ	R_L = 300 Ω, C_L = 35 pF;
		12	ns max	V_S = 3 V, Test Circuit 4
ADG733 $t_{ON}(\overline{EN})$	20		ns typ	R_L = 300 Ω, C_L = 35 pF;
		40	ns max	V_S = 3 V, Test Circuit 5
$t_{OFF}(\overline{EN})$	7		ns typ	R_L = 300 Ω, C_L = 35 pF;
		12	ns max	V_S = 3 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	13		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 3 V, Test Circuit 6
Charge Injection	±3		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth	160		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
C_S (OFF)	11		pF typ	f = 1 MHz
C_D, C_S (ON)	34		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital Inputs = 0 V or 5.5 V
		1.0	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	11	12	Ω max	Test Circuit 1
On Resistance Match between		0.1	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		3	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or 3 V;
	±0.1	±0.5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	28		ns typ	R_L = 300 Ω, C_L = 35 pF;
		55	ns max	V_S = 2 V, Test Circuit 4
t_{OFF}	9		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 2 V, Test Circuit 4
ADG733 $t_{ON}(\overline{EN})$	29		ns typ	R_L = 300 Ω, C_L = 35 pF;
		60	ns max	V_S = 2 V, Test Circuit 5
$t_{OFF}(\overline{EN})$	9		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 2 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	22		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 2 V, Test Circuit 6
Charge Injection	±3		pC typ	V_S = 1 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth	160		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
C_S (OFF)	11		pF typ	f = 1 MHz
C_D, C_S (ON)	34		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	0.001		µA typ	Digital Inputs = 0 V or 3.3 V
		1.0	µA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG733/ADG734–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +2.5 V ± 10%, V_{SS} = –2.5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA;
	4.5	5.0	Ω max	Test Circuit 1
On Resistance Match between		0.1	Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = –2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = +2.25 V/–1.25 V, Test Circuit 3
	±0.1	±0.5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		35	ns max	V_S = 1.5 V, Test Circuit 4
t_{OFF}	10		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 1.5 V, Test Circuit 4
ADG733 $t_{ON}(\overline{EN})$	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		40	ns max	V_S = 1.5 V, Test Circuit 5
$t_{OFF}(\overline{EN})$	10		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 1.5 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	13		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 1.5 V, Test Circuit 6
Charge Injection	±5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	–72		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
–3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
C_S (OFF)	11		pF typ	f = 1 MHz
C_D, C_S (ON)	34		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 2.75 V
I_{DD}	0.001		μA typ	Digital Inputs = 0 V or 2.75 V
		1.0	μA max	
I_{SS}	0.001		μA typ	V_{SS} = –2.75 V
		1.0	μA max	Digital Inputs = 0 V or 2.75 V

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to V_{SS} . . . . . 7 V
V_{DD} to GND . . . . . –0.3 V to +7 V
V_{SS} to GND . . . . . +0.3 V to –3.5 V
Analog Inputs[2] . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs[2] . . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . 100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . . 30 mA
Operating Temperature Range
Industrial (A, B Versions) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance . . . . . 150.4°C/W
20-Lead TSSOP, θ_{JA} Thermal Impedance . . . . . 143°C/W
16-Lead QSOP, θ_{JA} Thermal Impedance . . . . . 149.97°C/W
Lead Temperature, Soldering (10 sec) . . . . . 300°C
IR Reflow, Peak Temperature (<20 sec) . . . . . 235°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Overvoltages at A, EN, IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

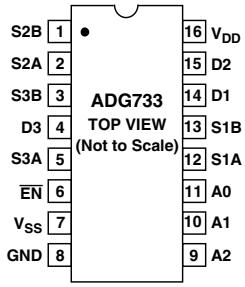
Model	Temperature Range	Package Description	Package Option
ADG733BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG733BRQ	–40°C to +85°C	Quarter Size Outline Package (QSOP)	RQ-16
ADG734BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20

CAUTION

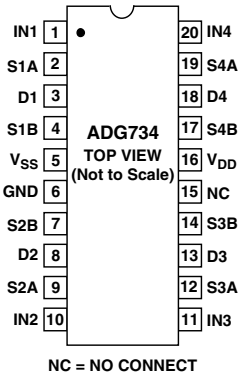
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG733/ADG734 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

TSSOP/QSOP



TSSOP



NC = NO CONNECT

Table I. ADG733 Truth Table

A2	A1	A0	$\overline{EN}$	ON Switch
X	X	X	1	None
0	0	0	0	D1-S1A, D2-S2A, D3-S3A
0	0	1	0	D1-S1B, D2-S2A, D3-S3A
0	1	0	0	D1-S1A, D2-S2B, D3-S3A
0	1	1	0	D1-S1B, D2-S2B, D3-S3A
1	0	0	0	D1-S1A, D2-S2A, D3-S3B
1	0	1	0	D1-S1B, D2-S2A, D3-S3B
1	1	0	0	D1-S1A, D2-S2B, D3-S3B
1	1	1	0	D1-S1B, D2-S2B, D3-S3B

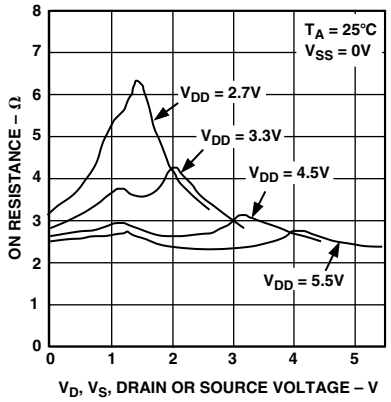
X = Don't Care.

Table II. ADG734 Truth Table

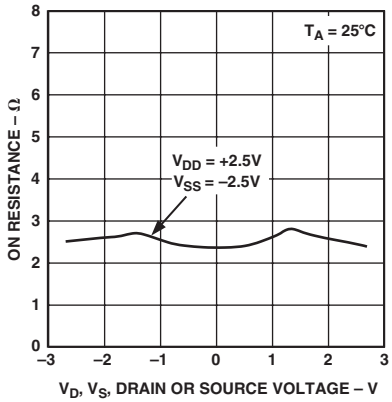
Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

TERMINOLOGY

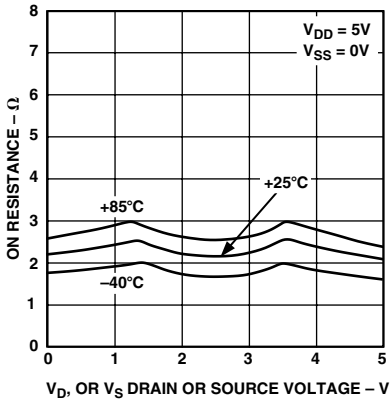
V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground close to the device.
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
A_X	Logic Control Input
$\overline{EN}$	Active low device enable
V_D (V_S)	Analog Voltage on Terminals D and S
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance Match between any Two Channels (i.e., R_{ON}max and R_{ON}min)
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF"
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON"
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
I_{INL}(I_{INH})	Input Current of the Digital Input
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D, C_S(ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance
t_{ON}	Delay Time Measured between the 50% and 90% Points of the Digital Inputs and the Switch "ON" Condition
t_{OFF}	Delay Time Measured between the 50% and 90% Points of the Digital Input and the Switch "OFF" Condition
$t_{ON}(\overline{EN})$	Delay Time between the 50% and 90% Points of the $\overline{EN}$ Digital Input and the Switch "ON" Condition
$t_{OFF}(\overline{EN})$	Delay Time between the 50% and 90% Points of the $\overline{EN}$ Digital Input and the Switch "OFF" Condition
t_{OPEN}	"OFF" Time Measured between the 80% Points of Both Switches when Switching from One Address State to Another
Charge	A Measure of the Glitch Impulse Transferred Injection from the Digital Input to the Analog Output during Switching
Off Isolation	A Measure of Unwanted Signal Coupling through an "OFF" Switch.
Crosstalk	A Measure of Unwanted Signal that Is Coupled through from One Channel to Another as a Result of Parasitic Capacitance
On Response	The Frequency Response of the "ON" Switch
Insertion Loss	The Loss Due to the On Resistance of the switch



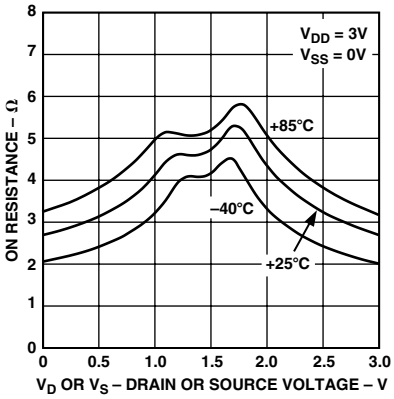
TPC 1. On Resistance as a Function of V_D (V_S) for Single Supply



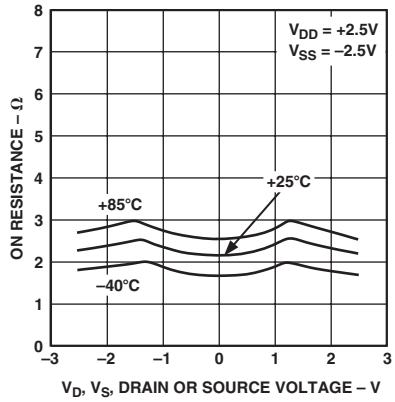
TPC 2. On Resistance as a Function of V_D (V_S) for Dual Supply



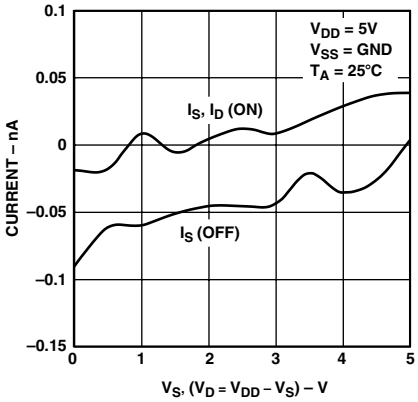
TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply



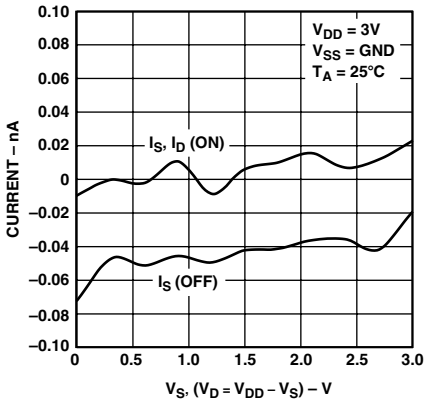
TPC 4. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply



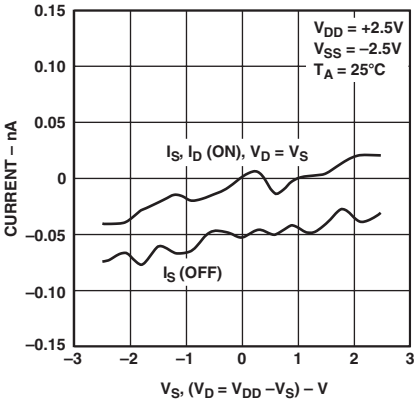
TPC 5. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply



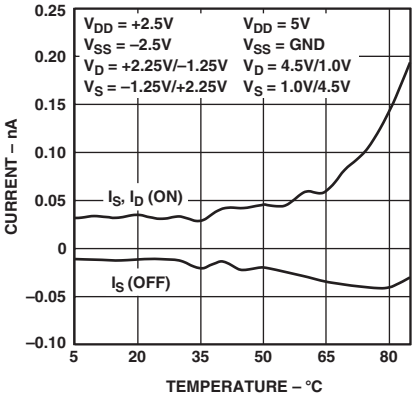
TPC 6. Leakage Currents as a Function of V_D (V_S)



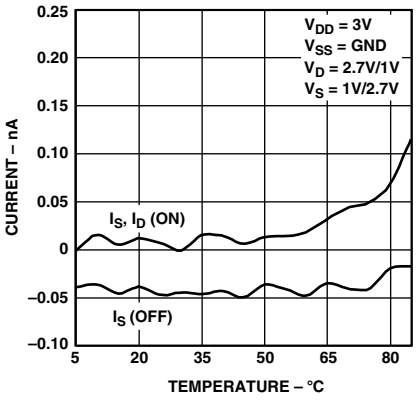
TPC 7. Leakage Currents as a Function of V_D (V_S)



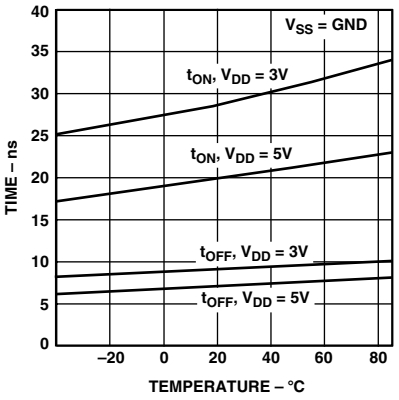
TPC 8. Leakage Currents as a Function of V_D (V_S)



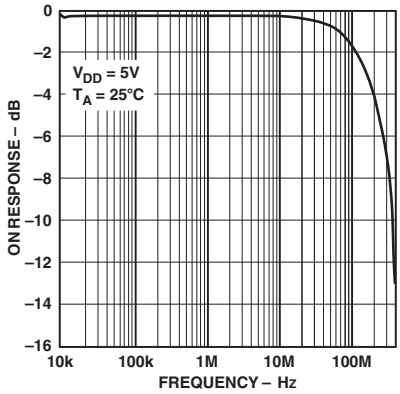
TPC 9. Leakage Currents as a Function of Temperature



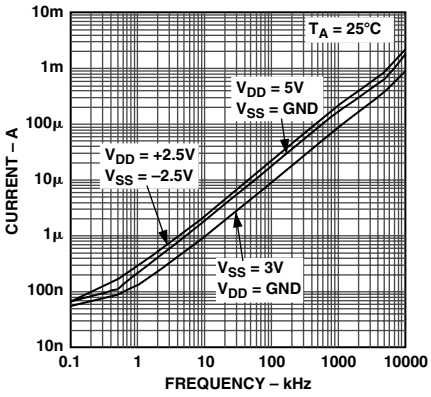
TPC 10. Leakage Currents as a Function of Temperature



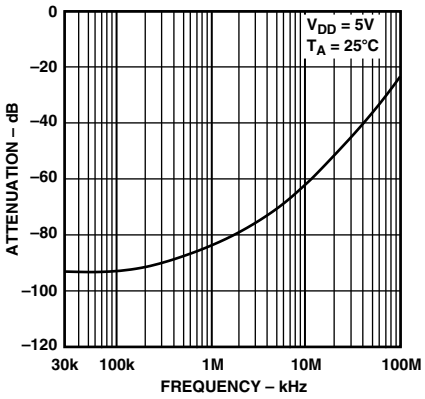
TPC 11. t_{ON}/t_{OFF} Times vs. Temperature



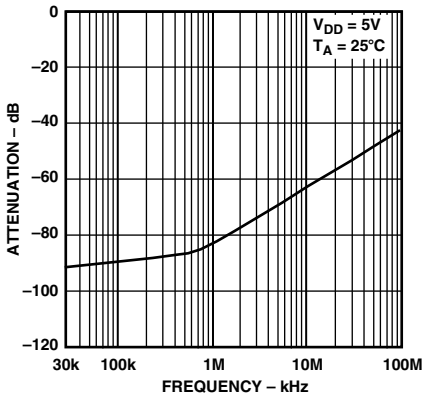
TPC 12. On Response vs. Frequency



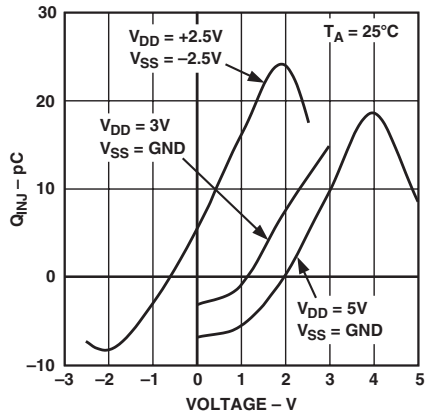
TPC 13. Input Current, I_{DD} vs. Switching Frequency



TPC 14. Off Isolation vs. Frequency

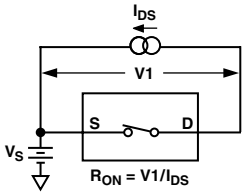


TPC 15. Crosstalk vs. Frequency

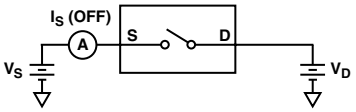


TPC 16. Charge Injection vs. Source Voltage

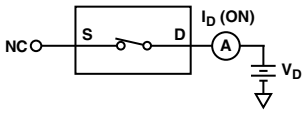
Test Circuits



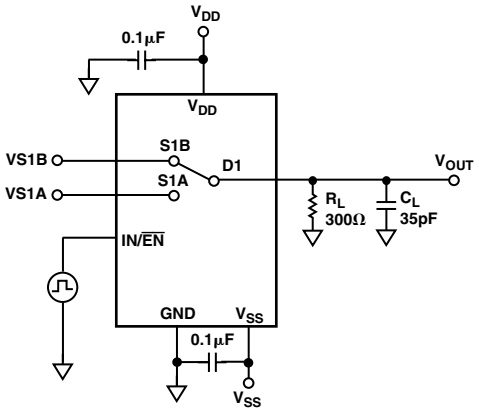
Test Circuit 1. On Resistance

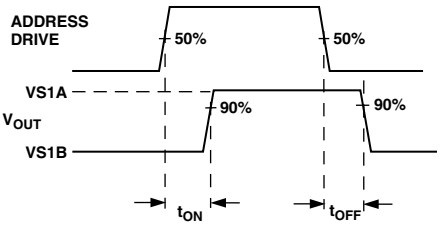


Test Circuit 2. I_S (OFF)

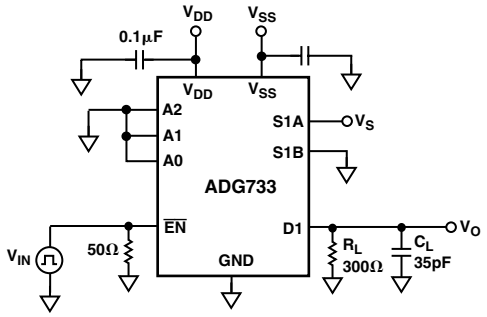


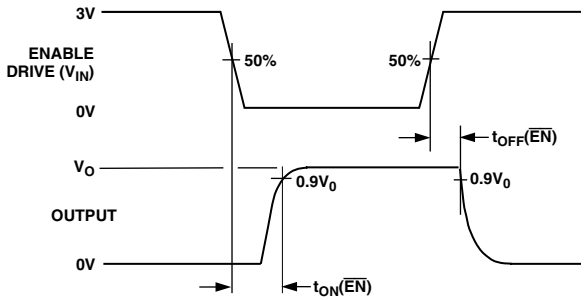
Test Circuit 3. I_D (ON)



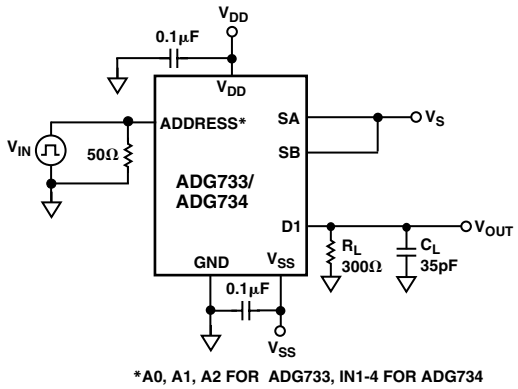


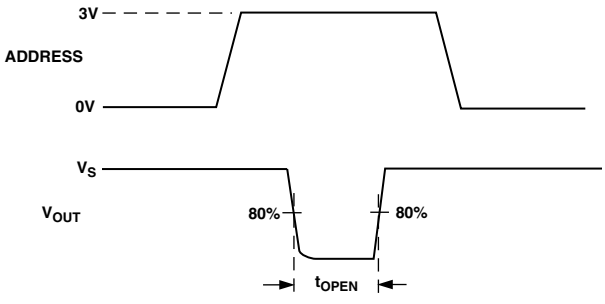
Test Circuit 4. Switching Times, t_{ON}, t_{OFF}



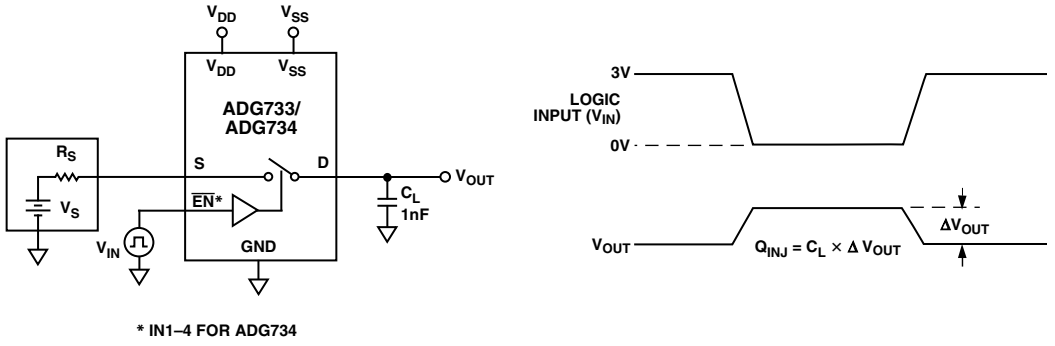


Test Circuit 5. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

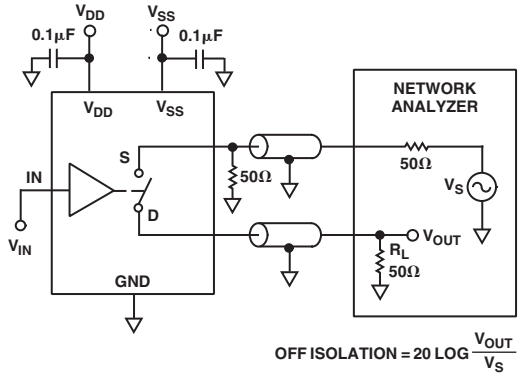




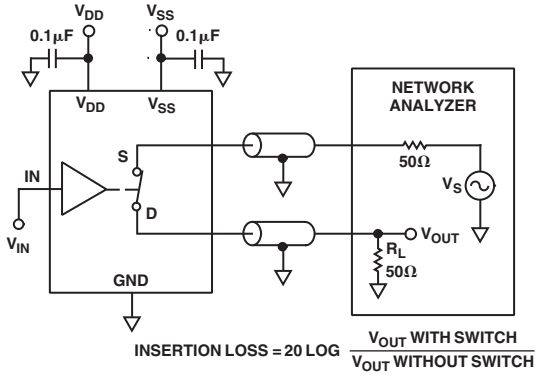
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



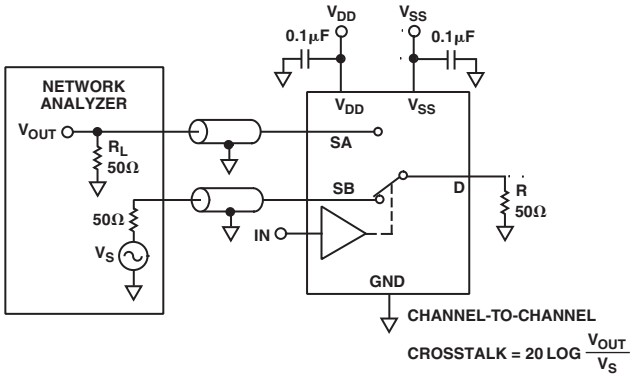
Test Circuit 7. Charge Injection



Test Circuit 8. Off Isolation



Test Circuit 10. Bandwidth

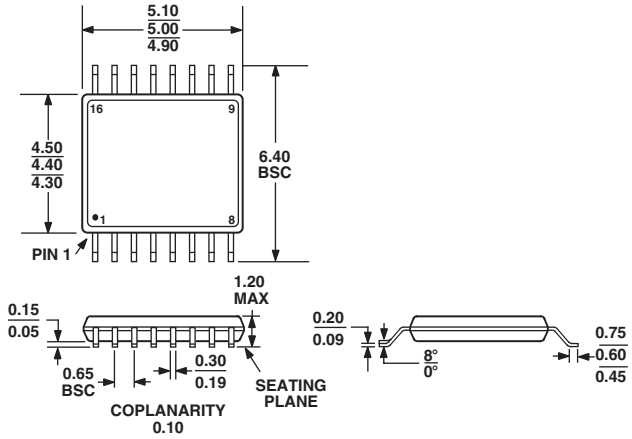


Test Circuit 9. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

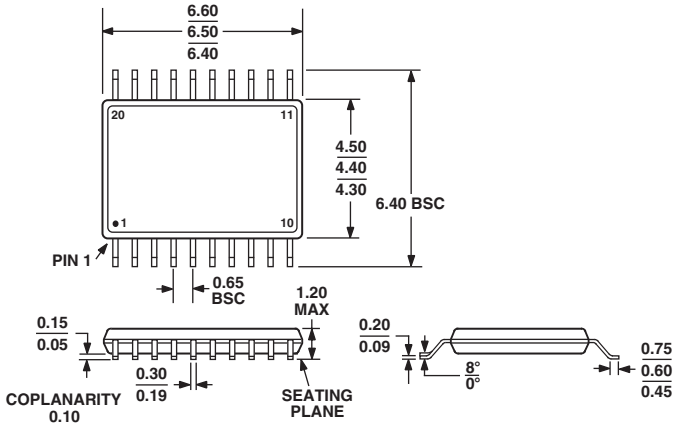
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB

20-Lead Thin Shrink Small Outline Package [TSSOP] (RU-20)

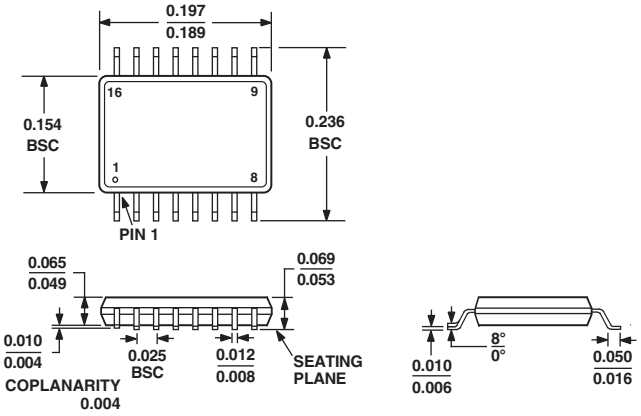
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AC

16-Lead SOIC, 0.025 Lead Pitch [QSOP] (RQ-16)

Dimensions shown in inches



COMPLIANT TO JEDEC STANDARDS MO-137AB

Revision History

Location	Page
11/02—Data Sheet changed from REV. 0 to REV. A.	
Changes to FEATURES	1
Changes to PRODUCT HIGHLIGHTS	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS Note 2	5
Changes to TERMINOLOGY table	6
Replaced TPCs 2, 5, 8, and 9	7
Edits to TPCs 6 and 7	7
Replaced TPC 12	8
Edits to TPCs 13 and 16	8
Replaced Test Circuits 8 and 9	10
Added Test Circuit 10	10
Updated OUTLINE DIMENSIONS	11

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